AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 14, 15 and 17 as shown below.

The following is a complete list of all claims in this application.

1-13. (Cancelled)

14. (Currently Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a gate line formed ~~in a horizontal direction~~ on the insulating substrate,

a gate insulating layer covering the gate line;

a data line formed ~~in a vertical direction~~ on the gate insulating layer;

an align pattern formed on the gate insulating layer and located on both sides of the data line;

a semiconductor pattern formed on the gate insulating layer;

~~a drain electrode formed on the semiconductor pattern,~~

~~a~~ source and drain ~~electrode~~ electrodes formed on the semiconductor pattern~~, the source electrode being separated from the drain electrode and connected to the data line~~;

a passivation layer covering the data line, the align pattern~~,~~ and the source and drain electrodes ~~electrode, and the source electrode~~, and having a contact hole exposing the drain electrode; and

a pixel electrode formed on the passivation layer and connected to the drain electrode through the contact hole.

15. (Currently Amended) The thin film transistor array panel of claim 14, further comprising an ohmic contact layer ~~layers~~ formed between the source and drain electrodes ~~electrode~~ and the semiconductor pattern~~, and between the drain electrode and the semiconductor pattern~~.

16. (Original) The thin film transistor array panel of claim 14, wherein the passivation layer and the gate insulating layer have an opening exposing the insulating substrate between the align pattern and the data line.

17. (Currently Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a gate line formed ~~in a horizontal direction~~ on the insulating substrate;

a gate insulating layer covering the gate line;

a data line formed ~~in a vertical direction~~ on the gate insulating layer;

an align pattern formed on the gate insulating layer and located on both sides of the data line;

a semiconductor pattern formed on the gate insulating layer;

~~a~~ source and drain electrodes ~~electrode~~ formed on the semiconductor pattern;

~~a source electrode formed on the semiconductor pattern, the source electrode being separated from the drain electrode and connected to the data line;~~

a pixel electrode formed on the gate insulating layer and connected to the drain electrode and the align pattern; and

a passivation layer covering the data line, the align pattern, the source and drain electrodes ~~electrode, the source electrode,~~ and the pixel electrode.

18-29. (Cancelled)